CLAIMS

This listing will replace all prior versions and listings of the claims in this application. Please amend the claims as listed below.

Listing of Claims:

Claims 1-30 (canceled)

31. (Previously presented): Apparatus for a bi-directional communication link having a plurality of channels, each of said channels comprising:

a master connected at a near end of the channel and a slave connected at an opposite end of the channel, said master comprising:

(a) a first transmitter coupled to the channel and having a master Tx clock signal; and

(b) a first receiver coupled to the channel and comprising:

(i) an analog-to-digital (A/D) converter that periodically samples a signal incoming over the channel to yield a received signal;

(ii) a clock recovery circuit that generates a master Rx clock from a clock signal embedded in the received signal; and

(iii) a metric processor, connected to an output of said A/D converter, that produces a metric signal reflective of amplitude differences between the received signal and allowed amplitude levels for the received signal; and

said slave comprising:

(a) a second receiver coupled to the channel and comprising a clock recovery circuit for generating a Slave Rx clock from a signal received over the channel and transmitted from the master;

(b) a second transmitter coupled to the channel and having a Slave Tx clock signal, said master Rx clock signal being frequency locked to said Slave Tx clock signal; and

(c) a first delay element for generating said Slave Tx clock signal by controllably delaying said Slave Rx clock signal; and

wherein said apparatus further comprises a decision processor, connected to said master and responsive to said metric signal, for determining a delay value to be

provided by said first delay element in the slave which will maximize the metric signal and issuing a command, via the first transmitter and the channel, to said second receiver in order to set a delay provided by said first delay element to said delay value, so as to reduce distortion caused by near end cross-talk and echo in signals received over the channel, by the first receiver and thus facilitate clock and data recovery by the first receiver.

32. (Previously presented): The apparatus of claim 31 further comprising, in the first receiver, a second delay element, situated between said Master Rx clock signal and said A/D converter and responsive to said decision processor, which controllably delays a sampling time, Ts, provided by said converter, wherein said decision processor independently sets the delays provided by the first and second delay elements in order to further maximize the metric signal.

33. (Previously presented): The apparatus of claim 32 wherein the metric processor comprises a processor for computing a proportion of samples of the received signal provided by the master falling within the allowed amplitude levels relative to those of said samples that fall outside of the allowed amplitude levels.

34. (Previously presented): The apparatus of claim 33 wherein said decision processor is connected to all the masters and is responsive to the metric signal produced in each of the masters so as to change the phase in each corresponding one of the slaves in order to maximize all the metric signals produced by all the masters.

35. (Previously presented): The apparatus of claim 31 wherein said decision processor is connected to all the masters and is responsive to the metric signal produced in each of the masters so as to change the phase in each corresponding one of the slaves in order to maximize all the metric signals produced by all the masters.

36. (previously presented): The apparatus of claim 31 wherein the metric processor comprises a processor for computing a proportion of samples of the received signal

provided by the master falling within the allowed amplitude levels relative to those of said samples that fall outside of the allowed amplitude levels.

37. (previously presented): The apparatus of claim 36 wherein said decision processor is connected to all the masters and is responsive to the metric signal produced in each of the masters so as to change the phase in each corresponding one of the slaves in order to maximize all the metric signals produced by all the masters.

38. (previously presented): Apparatus for a bi-directional communication link having a plurality of channels with a master and a slave at respective ends of each one of the channels so as to define respective pluralities of masters and slaves, the master issuing a Master Tx clock, the slave constructing both a Slave Rx clock frequency-locked to the Master Tx clock and a Slave Tx clock frequency-locked to the Slave Rx clock, said apparatus comprising:

a metric processor, situated within said master, which produces a metric signal reflective of amplitude differences between a signal received by the master from a corresponding one of the slaves and allowed amplitude levels of the received signal; and

a decision processor, connected to the master and responsive to the metric processor, for changing phase of the Slave Tx clock relative to the Slave Rx clock in the corresponding one of the slaves in order to maximize the metric signal produced by the metric processor and thereby reduce distortion caused by near end cross-talk and echo in signals received over the channel by a receiver in the master and thus facilitate clock and data recovery by the receiver.

39. (previously presented): The apparatus of claim 38 wherein said metric processor comprises a processor for computing a proportion of samples of the received signal provided by each of said masters and which fall within the allowed amplitude levels relative to those ones of said samples that fall outside of the allowed amplitude levels.

40. (currently amended): The apparatus of claim ~~34~~ 38 wherein said decision processor is connected to all the masters and is responsive to the metric signal

produced in each of the masters so as to change the phase in each corresponding one of the slaves in order to maximize all the metric signals produced by all the masters.

41. (previously presented): The apparatus of claim 38 wherein said decision processor is connected to all the masters and is responsive to the metric signal produced in each of the masters so as to change the phase in each corresponding one of the slaves in order to maximize all the metric signals produced by all the masters.